

FIGURE 2

FIG. 3

15

5e

5f

5

FIGURE 3

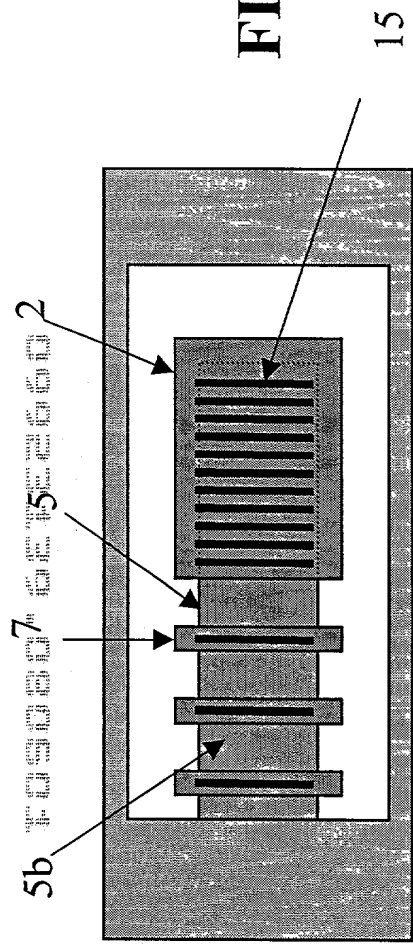


FIGURE 4(a)

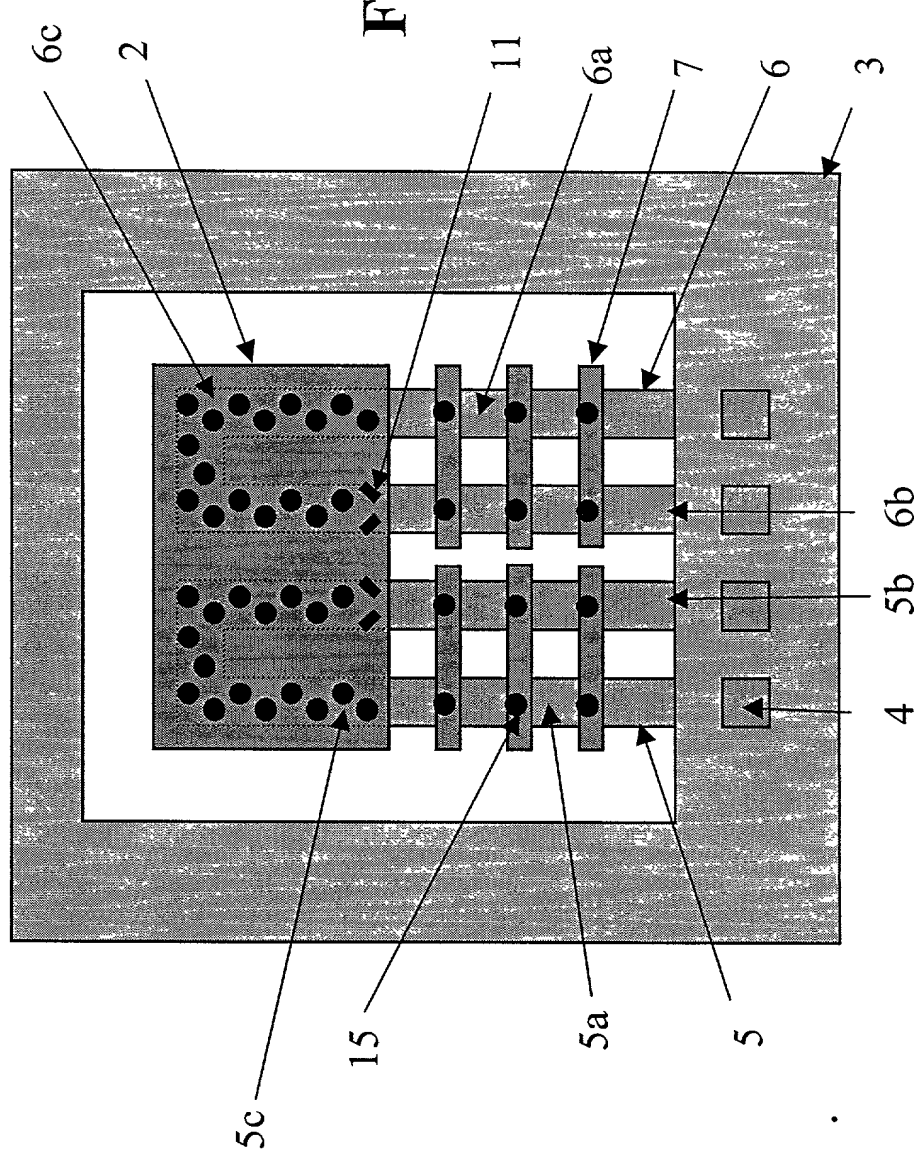
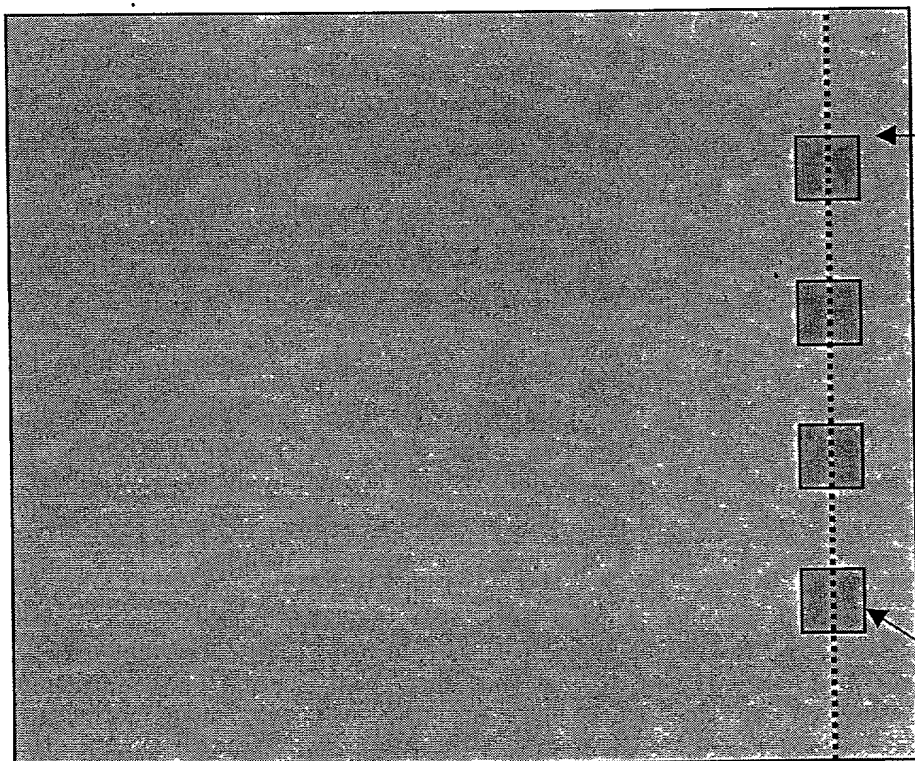


FIGURE 4(b)

FIG. 5 is a schematic diagram of a device 100 in accordance with the present invention. The device 100 includes a substrate 101, a first layer 102, a second layer 103, and a third layer 104. The first layer 102 is formed on the substrate 101, and the second layer 103 is formed on the first layer 102. The third layer 104 is formed on the second layer 103, and includes a plurality of openings 105. The openings 105 are formed in the third layer 104, and are in communication with the first layer 102. The openings 105 are formed in the third layer 104, and are in communication with the first layer 102. The openings 105 are formed in the third layer 104, and are in communication with the first layer 102.



104 **FIGURE 5(a)** 103

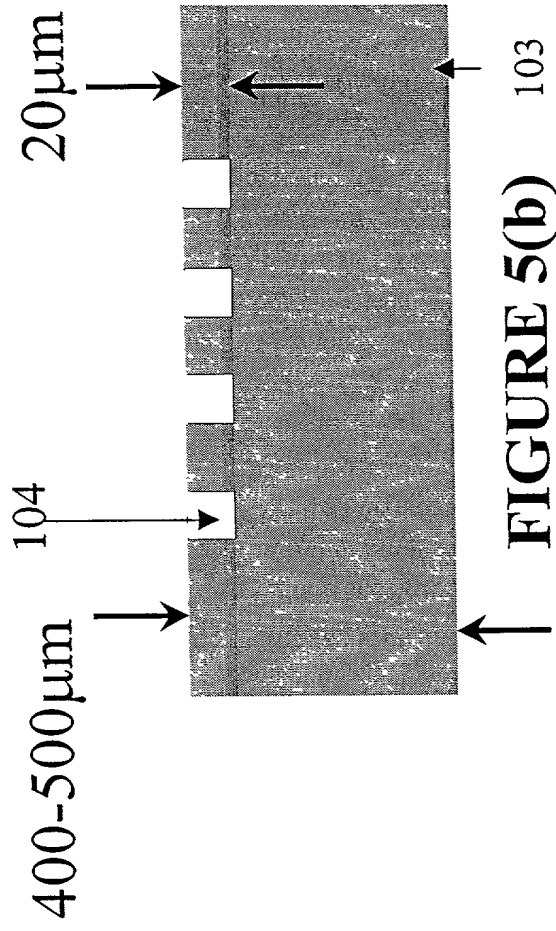


FIGURE 5(b) 103

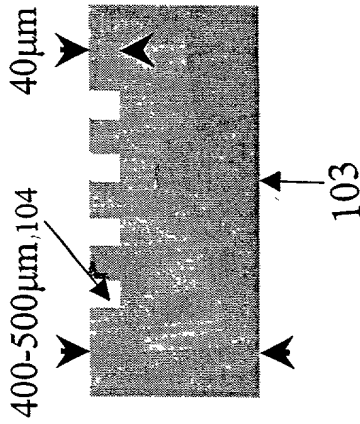
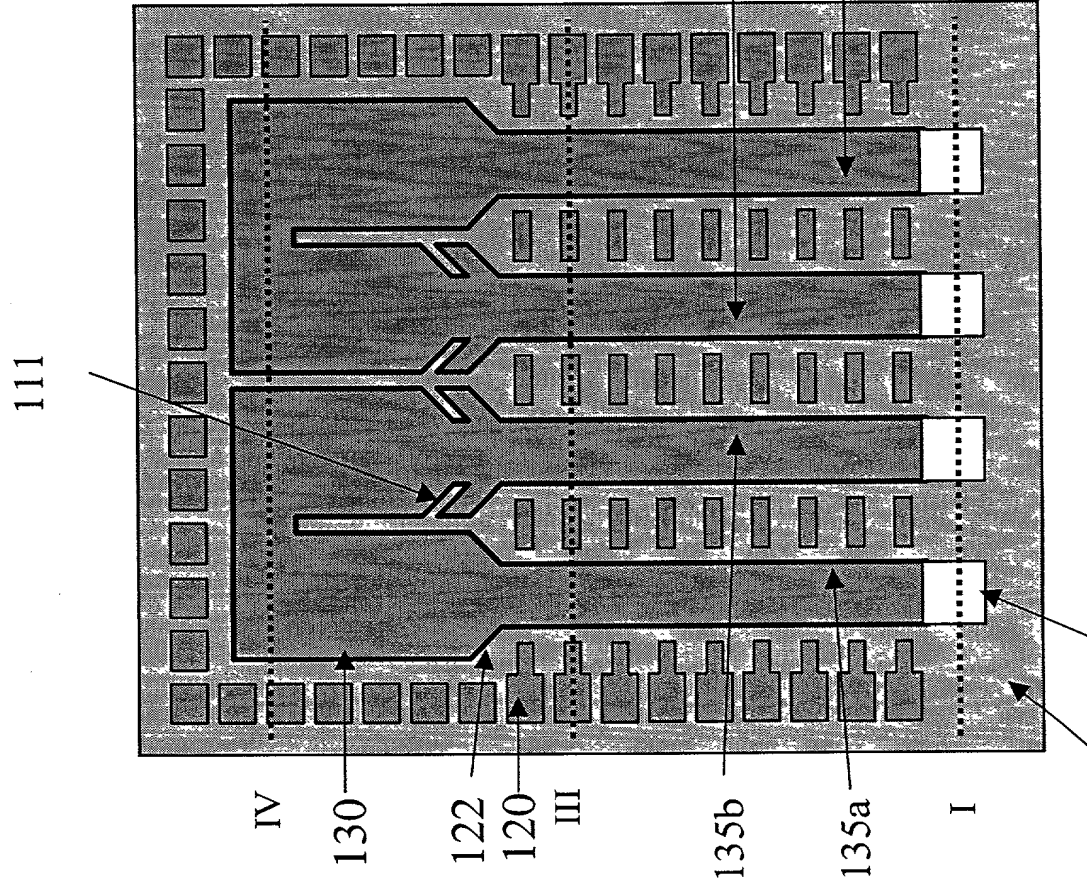


FIGURE 5(c) 103



103 104 **FIGURE 5(f)**

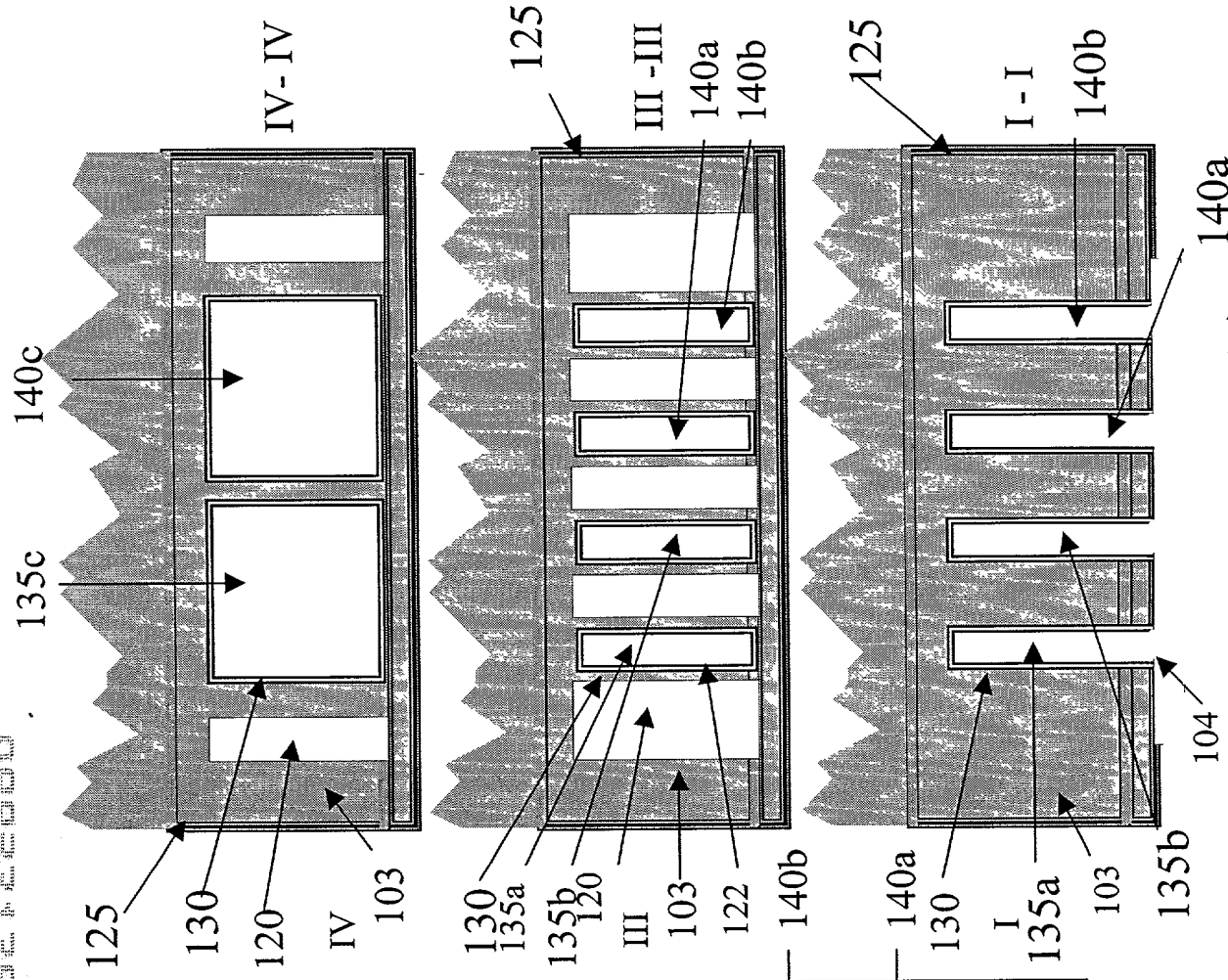


FIGURE 5(g)

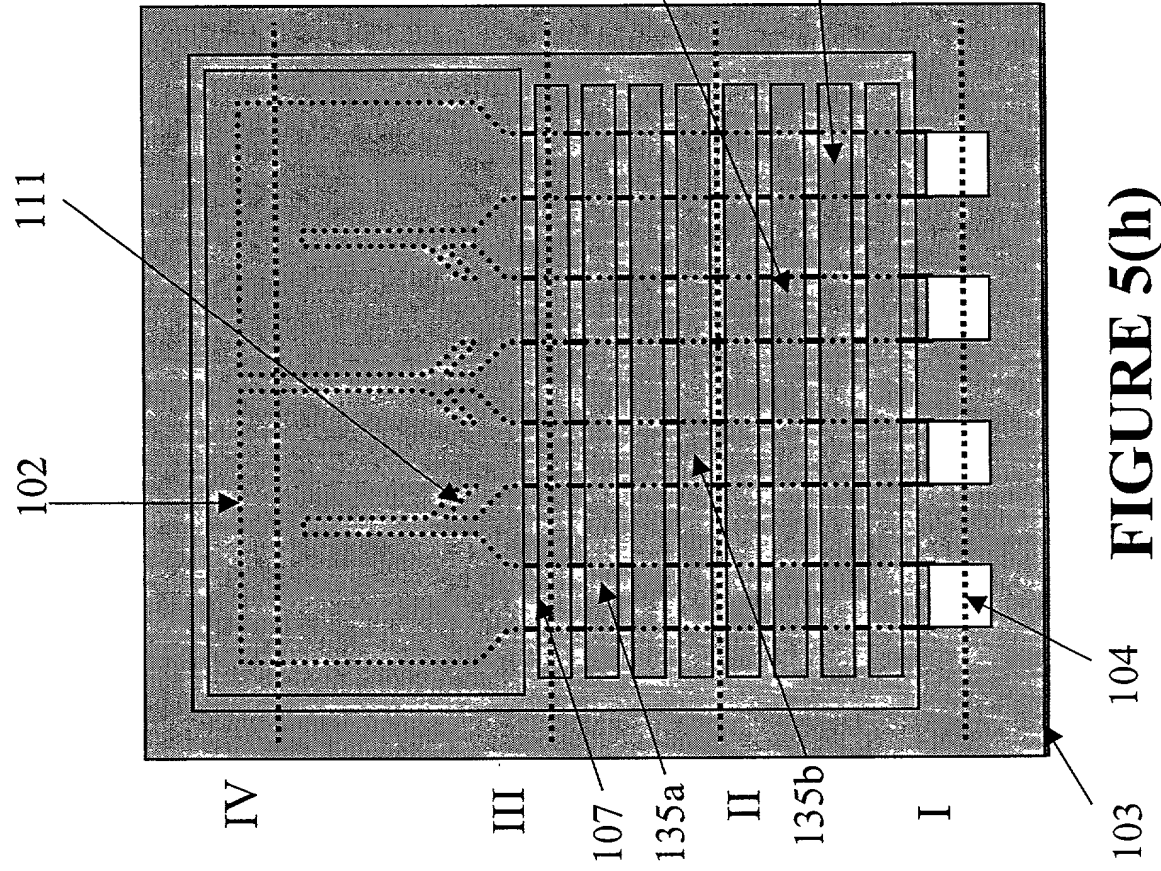


FIGURE 5(h)

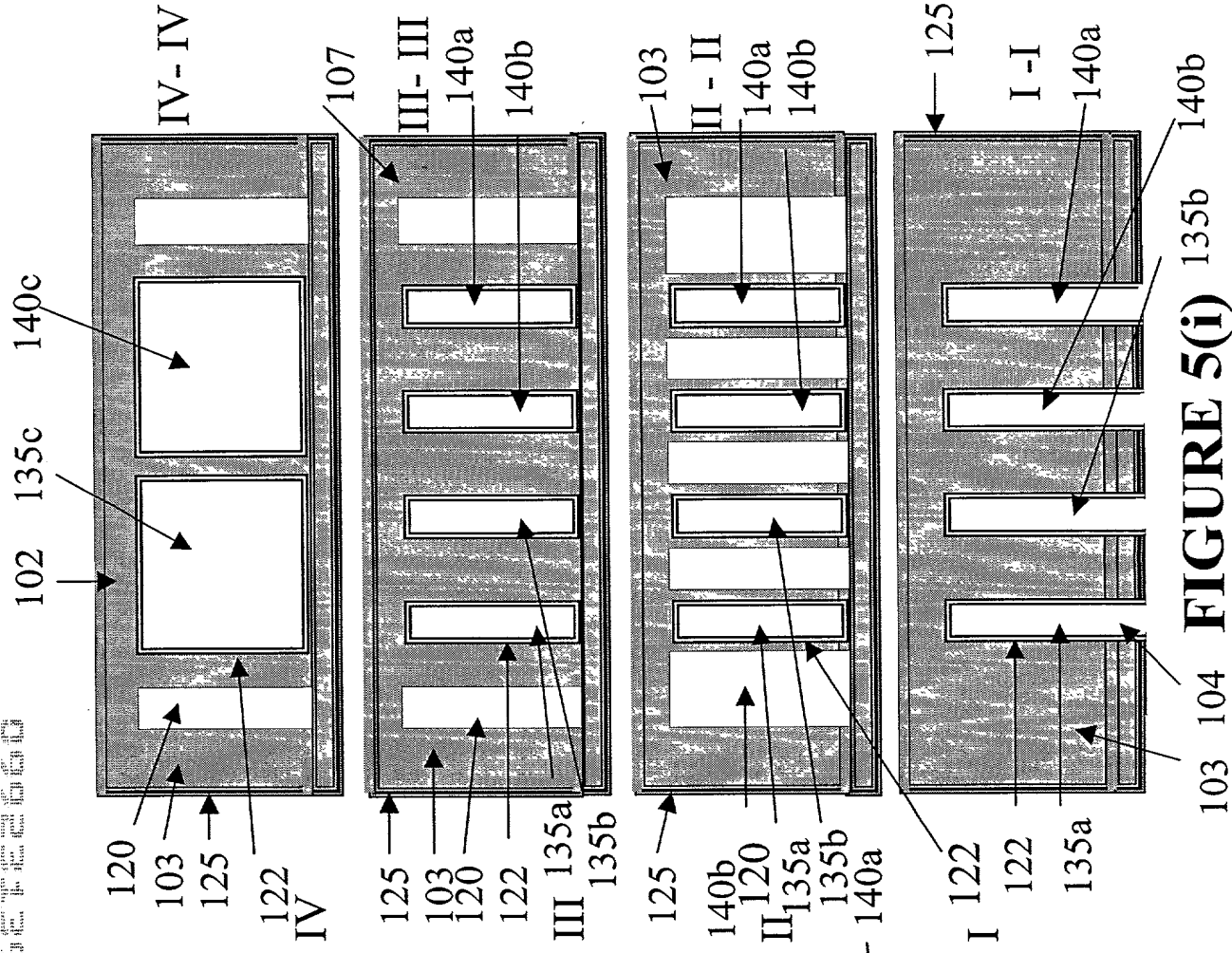
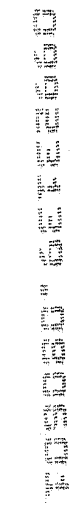


FIGURE 5(i)



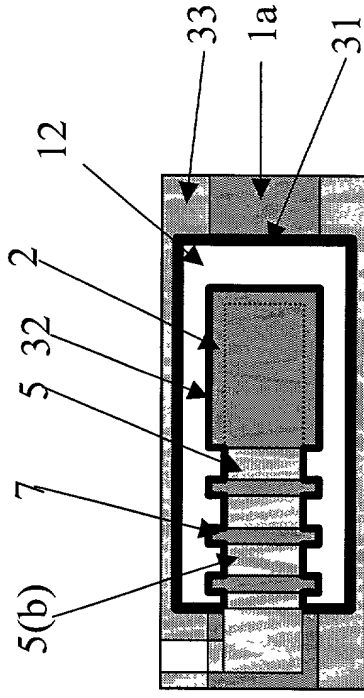


FIGURE 6(b)

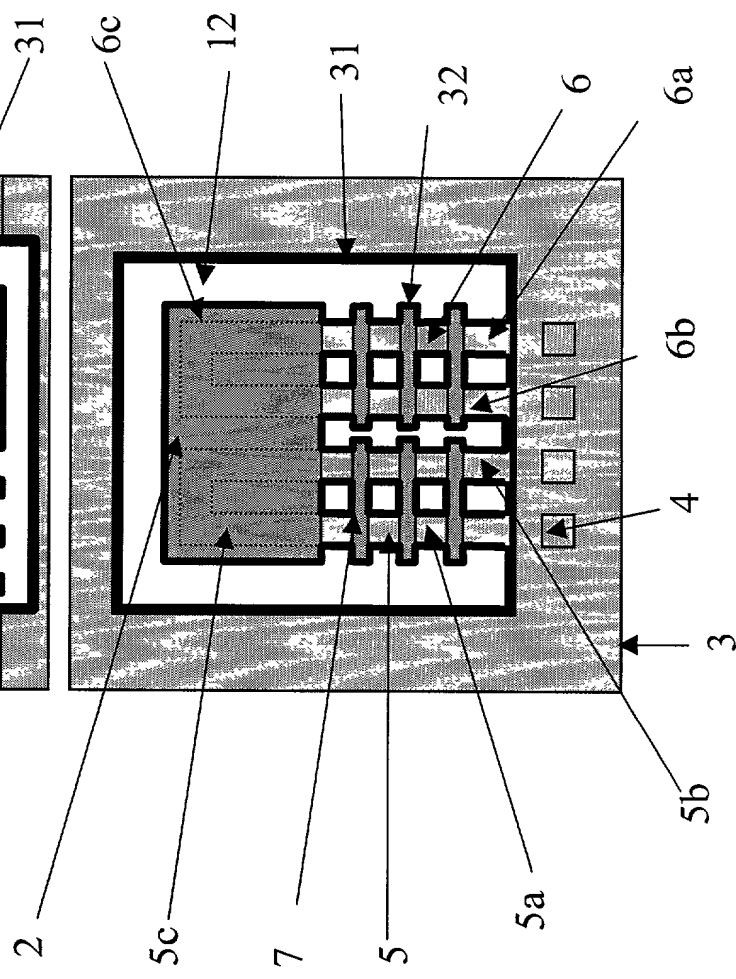


FIGURE 6(a)

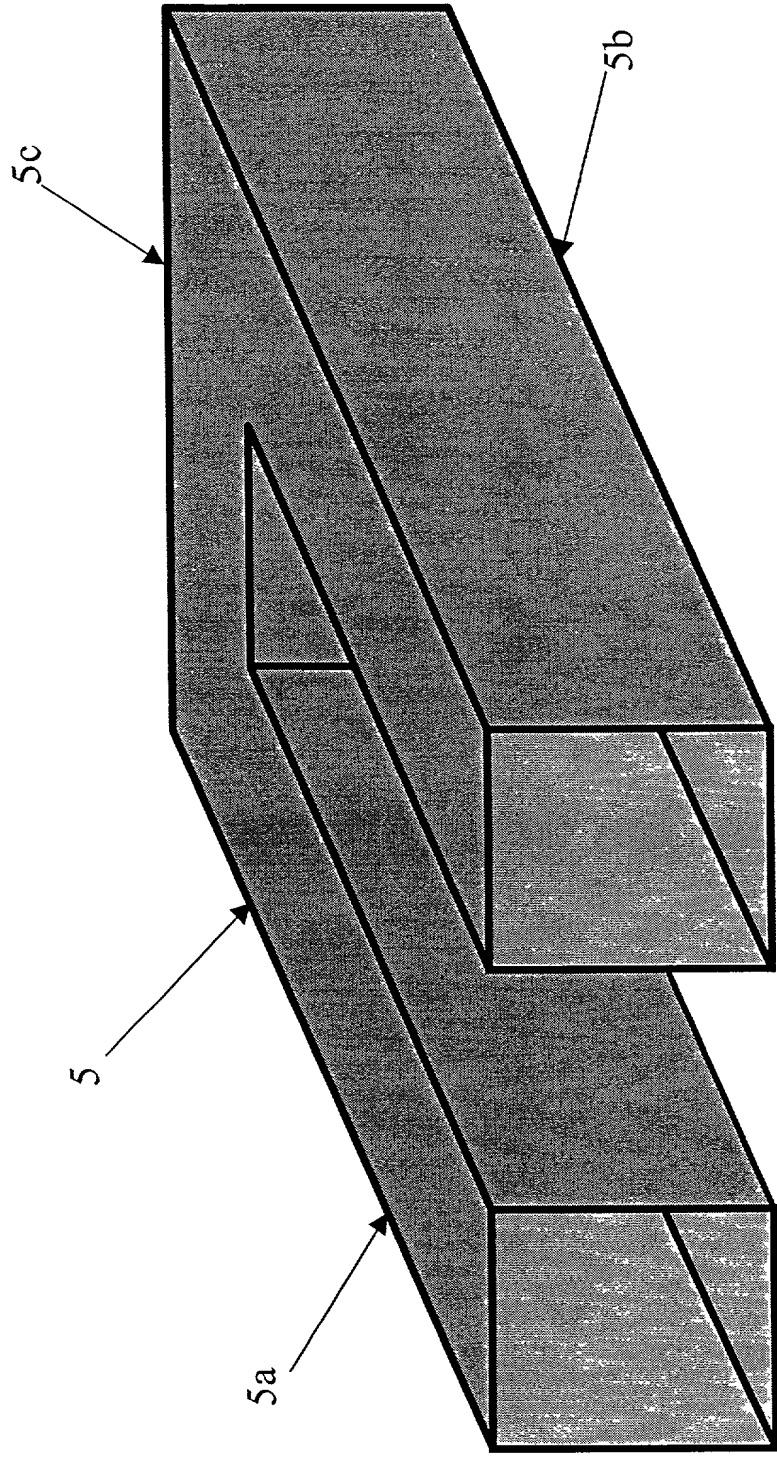
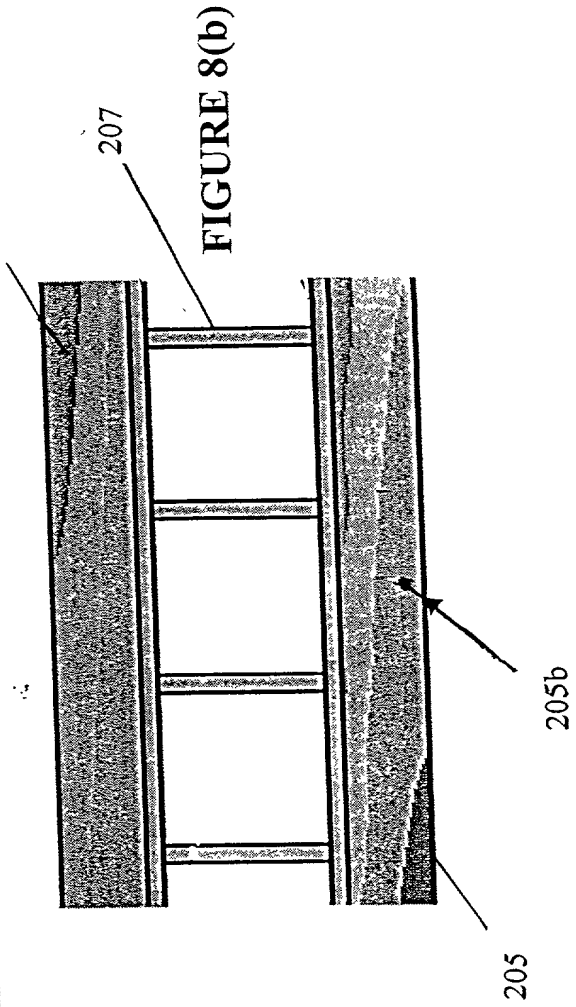
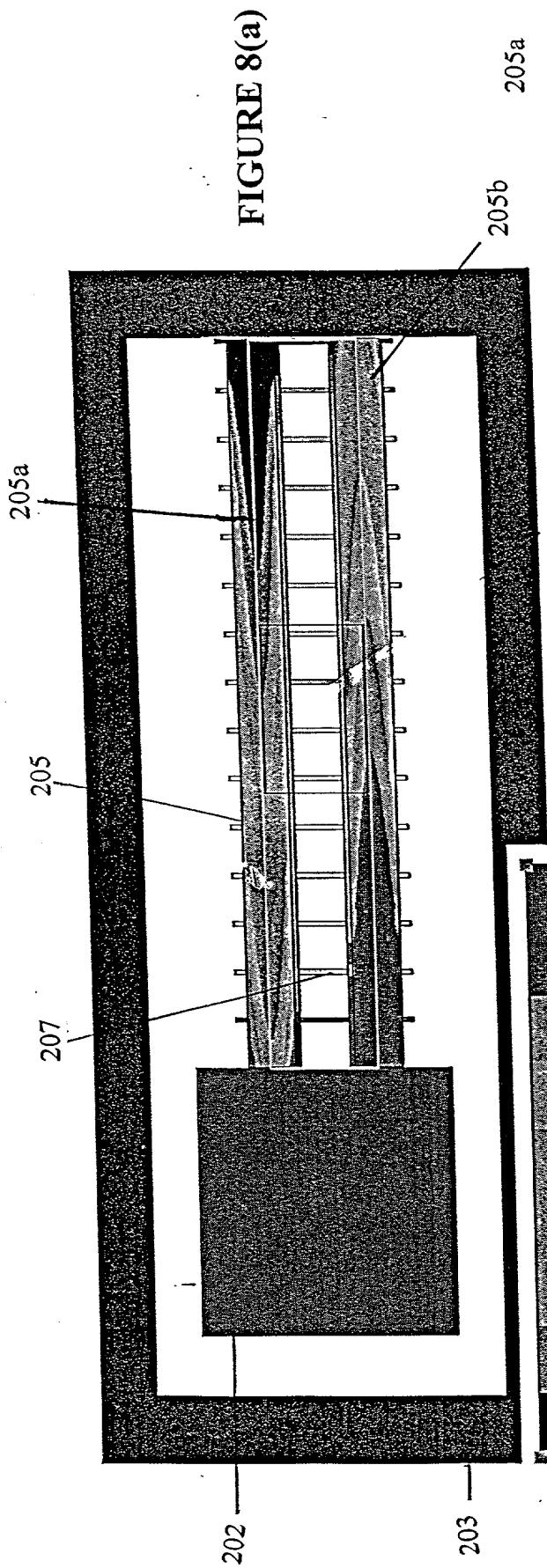
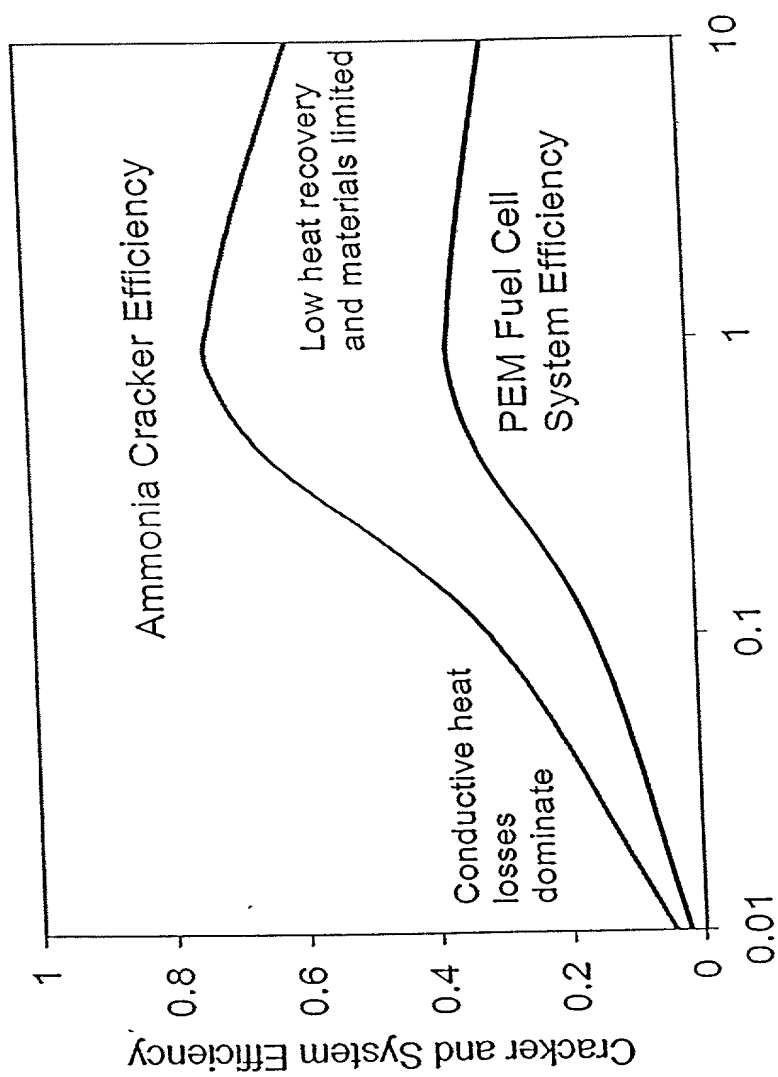


FIGURE 7





System Power Output (w)

FIGURE 9

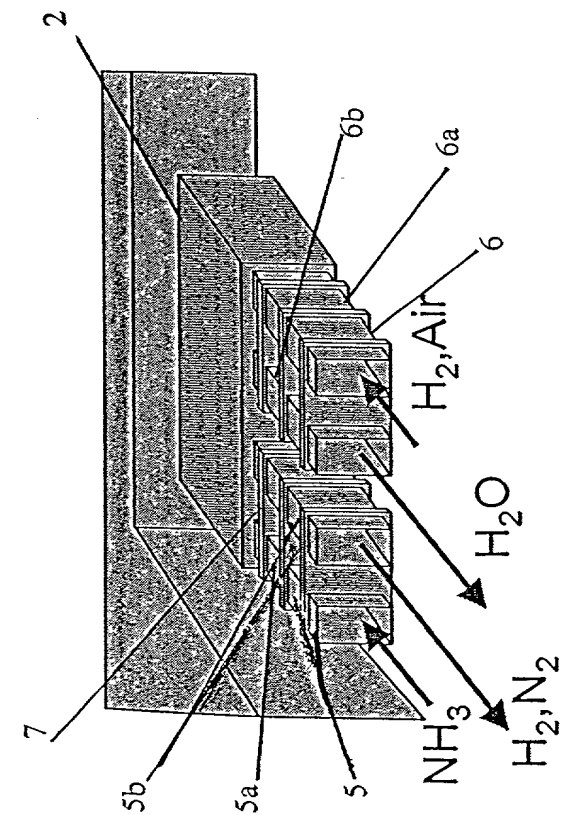


FIGURE 10(a)

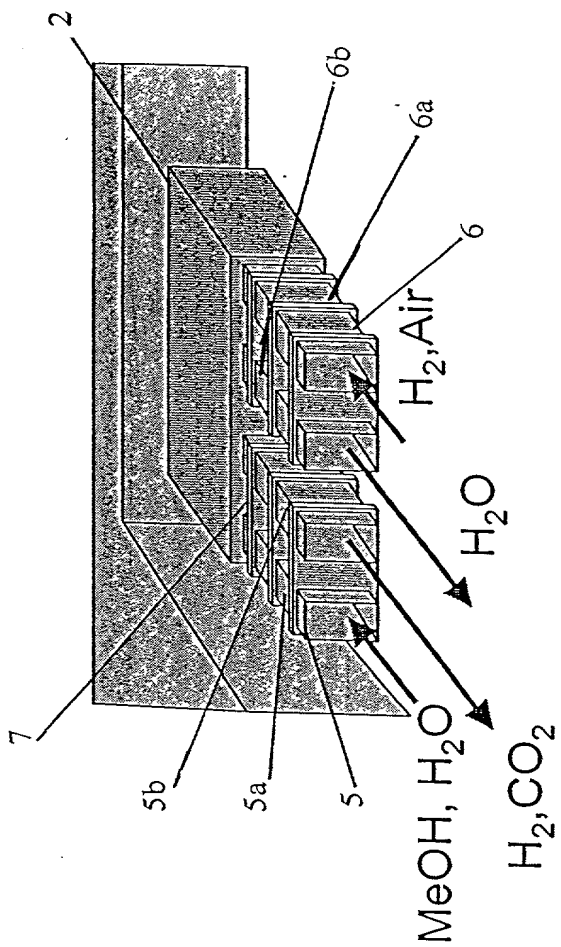


FIGURE 10(b)

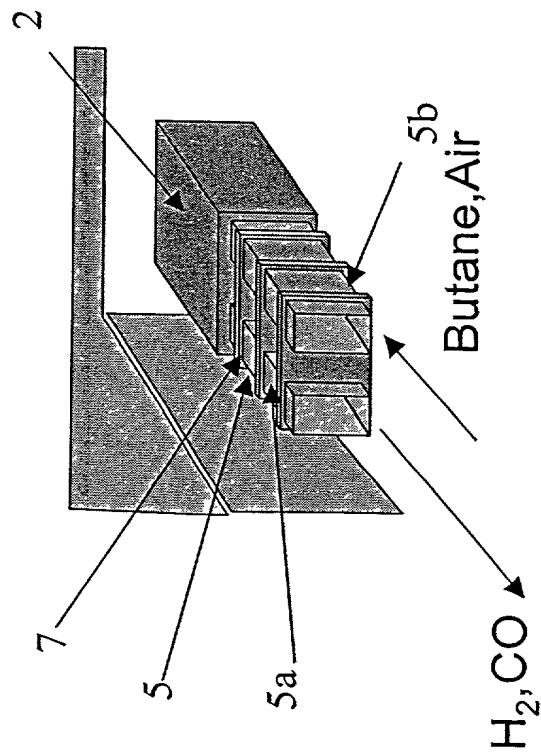
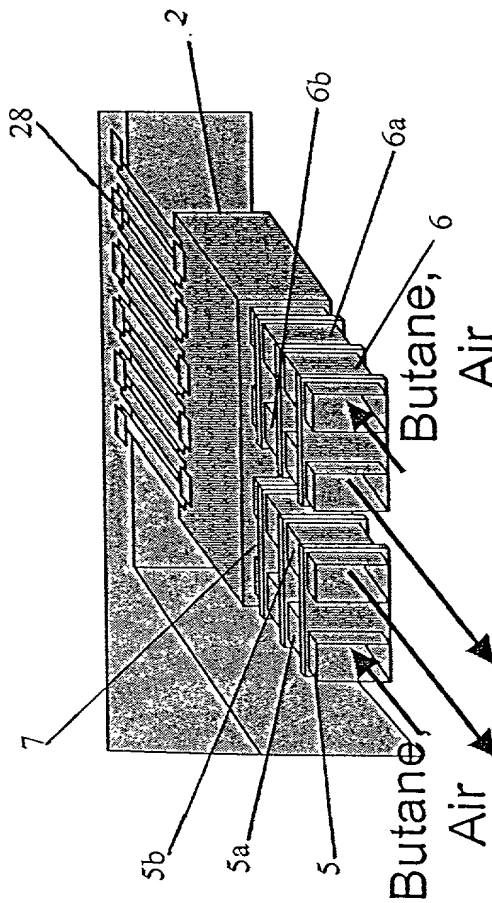


FIGURE 10(c)



H₂O, FIGURE 10(d)

CO₂

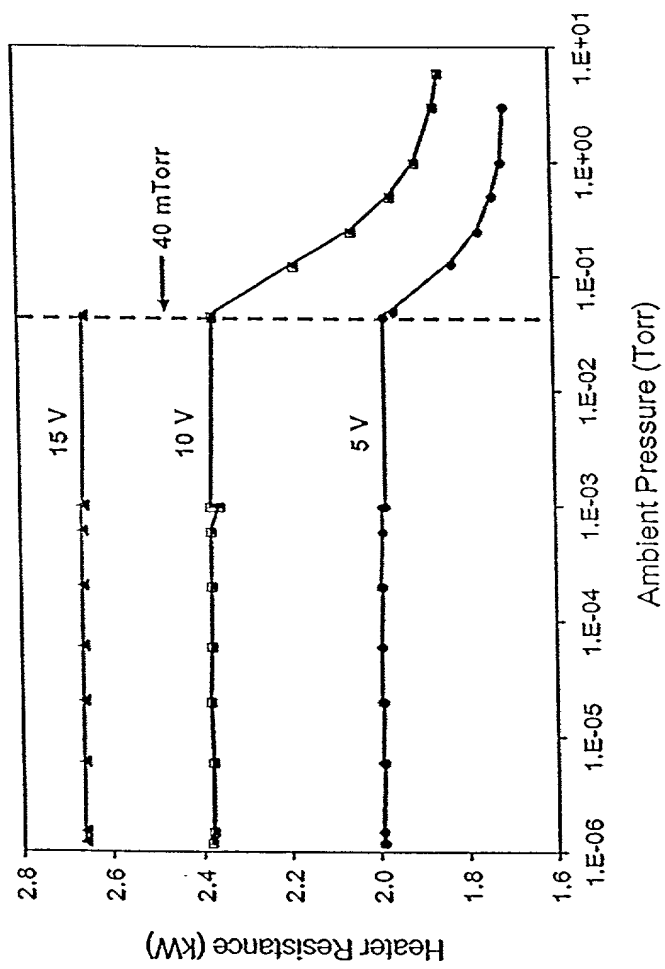


FIGURE 11

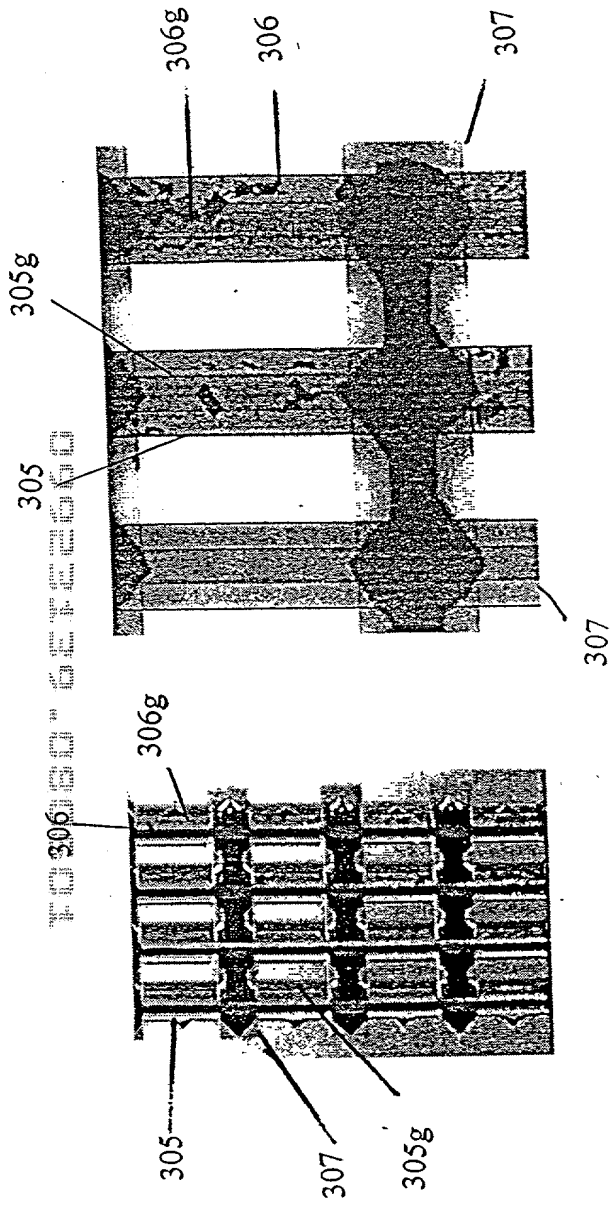


FIGURE 12(a)

FIGURE 12(b)

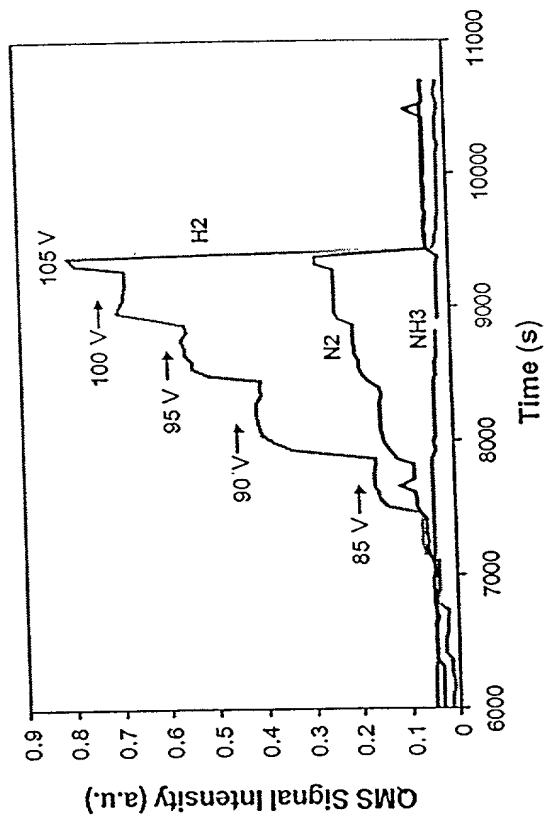


FIGURE 12(c)

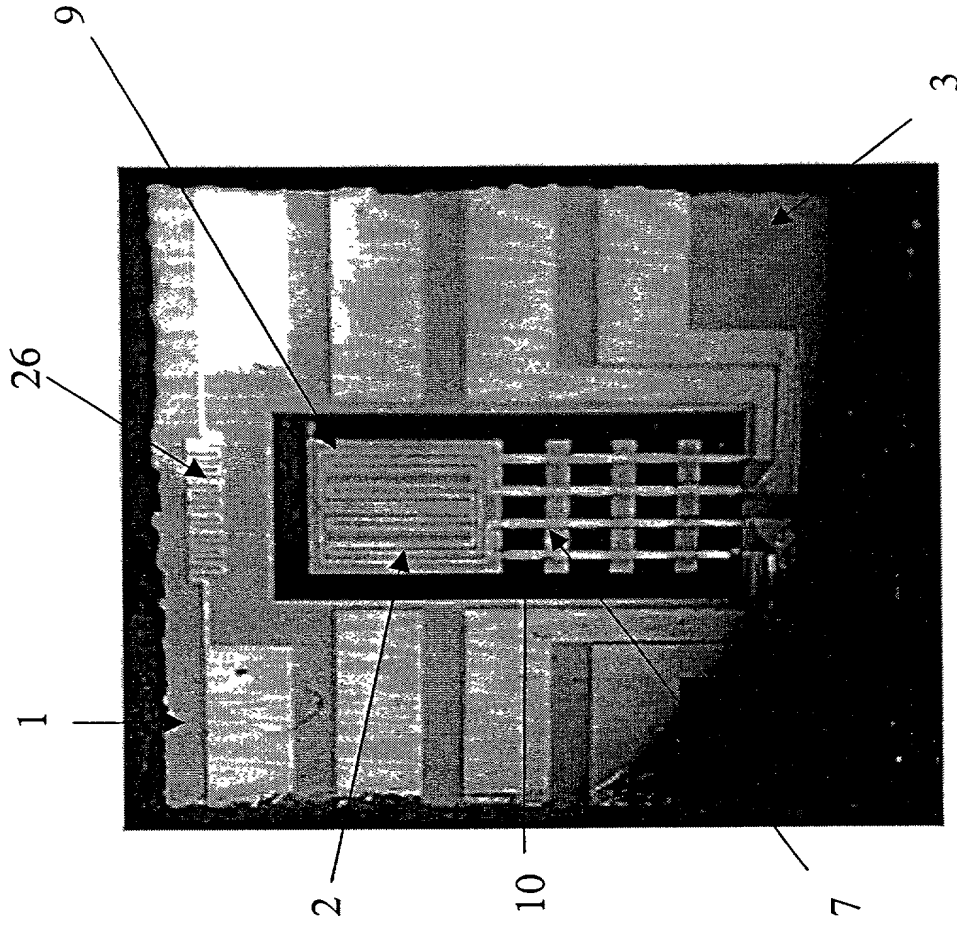


FIGURE 13(b)

FIGURE 13(a)